

满坤电子有限公司 MANKUN ELECTRONIC CO., LTD.

PCB 线路设计・制・造・高 Professional PCB design and manufacture

MANKUN



DEVELOPMENT AND DESIGN OF PROFESSIONAL PCB

专业PCB开发与设计

THINGS TO CONSIDER WHEN DESIGNING CIRCUI

Many factors come into play in circuit design with respect to etching, surface finishing and mechanical fabrication processes; such as holes, flatness, singulation and tolerances.

Fabrication of aluminum copper cladlaminates is similar to traditional FR-4 circuit boards with regard to imaging and wet processing operations. Mankun, secondary mechanical operations are unique, so the consideration of specific design recommendations are critical to ensure the manufacture of reliable, cost-effective aluminum copper cladlaminates circuits. This white paper will address design recommendations for circuit image, soldermask, legend and mechanical fabrication. Additional consideration for trace widths, spacing and clearances may be required for electrical integrity based on application voltage.

电路设计时要考虑的问题

在电路设计中,涉及到蚀刻、表面工艺和机械制造过程有关的因素很多,例如孔、平整度、V割和公差等。

在显影和蚀刻处理操作,铝基覆铜箔层压板的制造与传统FR-4电路板相似。但是,二次机械操作是唯一的,因此考虑特定的设计建议,对于确保制造可靠的、具有成本效益的铝基覆铜箔层压板电路是至关重要的。我们将针对电路图像、阻焊层、丝印和机械制造提出设计建议。对于基于施加电压的电气完整性,可能还需要额外考虑迹线宽度、间距和间隙。





Checklist To Optimal Design	优化设计项目
Ideas For Minimizing Cost (P2)	降低成本方法
Submit Appropriate File Types (P2)	提交适当的文件类型
Circuit Design (P3)	电路设计
Part Fabrication Methods (P3-P5)	PCB制作方法
Testing Options (P6)	测试选项
Advanced Circuit Processing (P6)	高级电路处理
Two-Layer Design Considerations (P7)	双层设计注意事项
Designing A Non-Rectangular Part Array (P8)	设计非矩零件阵列
Circuit Design Standards (P9-P10)	电路设计标准
Legend Design Standards (P9-P10)	图例设计标准
Soldermask Design Standards (P9-P10)	阻焊膜设计标准
Surface Finish Standards (P9-P10)	表面粗糙度标准
Mechanical Design Standards (P9-P10)	机械设计标准

Acceptable File Types For Design Submission 设计提交可接受的文件类型

- 1.Preferred data format Gerber RS274X include all layers (with embedded aperture list). DXF and some other formats are acceptable but take time to convert to Gerber and may become corrupted in the conversion process.
- Provide mechanical print with part and array dimensions (if applicable), identify material, soldermask type and color and surface finish.
- 3. Identify areas of possible design violation.
- 4. Include operating voltage and maximum operating temperature.
- 5. Include engineering or circuit design contact information.
- 1.首选的数据格式Gerber -包括所有层(具有嵌入式光圈列表). DXF和某些其他格式是可以接受的,但是转换到Gerber需要花费一些时间。并且在转换过程中可能会损坏。
- 2.提供具有零件和阵列尺寸(如果适用)的机械印刷,标识材料, 阻焊层类型以及颜色和表面光洁度。
- 3.确定可能违反设计的区域。
- 4.包括工作电压和最高工作温度。
- 5.包括工程或电路设计联系信息。

COST-EFFECTIVE BASIC MATERIALS FOR AN OPTIMAL DESIGN

具有成本效益的基础材料, 可实现最佳设计

Ideas For Minimizing Cost

降低成本的方法

Material Stack-Up - 5052 aluminum is the most cost effective base material. 6061-T6 aluminum is also available for applications which utilize the aluminum as a base for retaining fasteners or when considering specific fabrication applications.

Base Material Thickness - Using standard gauges will help control cost. Most common standard aluminum thicknesses are 1.0mm (0.040'') and 1.6mm (0.062'') and standard copper is 1.0mm (0.040''). Other thicknesses are also available.

Dielectric - The majority of applications are able to utilize our MP (multi-purpose) dielectric. If your application requires higher thermal performance or dielectric strength, please reference our characteristics of dielectric summary within our tclad Selection Guide..

材料规格 5052铝是最具成本效益的基础材料。 6061-T6铝也可用于以铝为基础固定紧固件的应用, 或在考虑特定制造应用时使用。

常规材料厚度: 使用标准量规将有助于控制成本。 最常见的标准铝厚度为1.0mm和1.6mm,标准铜为 1.0mm。其他厚度也可提供。

电介质-大多数产品应用都能够利用. 我们的金属基板热传导率数值表可以供参考.

■ Numerical table of heat conductivity of metal substrate 金屬基板熱傳導率數值表

Product name 品 名		Power substrate 電源基板			LED Lighting/car Lighting L E D照明/車截照明		
Insulation type 絕緣层种类		Low dielectric 低介電		High heat dissipat 高散熱		tion	hypoelasticity 低弹性
Insulation thickness 絕緣层厚度(µm)		80	125	125	125	80	100
Copper foil thickness 網箔厚度(μm)		35	70	70	70	70	70
peel strength 剥离强度(N/cm)		18	20	21	20	20	13
Interspace voltage resistance —分間耐電壓(kv)		2	5	4.5	4	2	2.5
Insulation failure voltage 經緣破壞電壓(kv)		5	7	6	6	4	6
Volume resistance 體積電阻(Ωcm)	me resistance 體積電阻(Ωcm)		5X10 ¹⁵		4X10 ¹⁵		
Dielectric constant 介電常數	1MHZ	4.5	4.6	7.2	7.8	7.8	4.3
Thermal resistance 熱阻(*C/W)	NSK method NSK	0.5	0.65	0.55	0.35	0.25	0.5
Thermal conductivity熱傳導率(W/mk)	*1	1	1.5	2.0	3.0	3.0	1.5
Solder heat resistance 焊料耐熱性	300℃	>10 points(分) >2 points(分)			>2 points(分)		
Glass transition point 玻璃轉化點(°C)	*2:DSC *3:DMS	160 ^{*2}	170 ^{*2}	155 ^{*2}	155 ^{*2}	155 ^{*2}	60 ^{*3}

*根據ASTM E 1530標准 ■ 以上歌儀是刑試相對值、並非絕



CIRCUIT DESIGN

电路设计

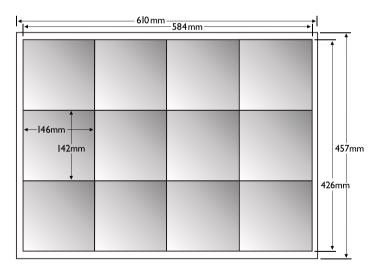
Material Utilization

Independent of the fabrication method chosen, square or rectangular designs will utilize the material most efficiently. The usable area of an 457 x 610mm (18.0" x 24.0") panel is 432 x 584mm (17.0" x 23.0"), for a 508 x 610mm (20.0" x 24.0") panel it is 483 x 584mm (19.0" x 23.0") and for a 457 x 635mm (18.0" x 25.0") panel it is 432 X 610mm (17.0" X 24.0"). For best cost value, maximize use of this usable area. The shape of the part effects cost, so please reference the section on part singulation for helpful guidelines.

材料的利用率

与选择的制造方法无关,正方形或矩形设计将最有效地利用材料。457*610mm尺寸的可用区域为432*584mm,508*610mm尺寸的可用区域为483*584mm,而457*635mm尺寸的可用区域是432*610mm,为了获得最佳成体价值,请充分利用该可用区域。零件的形状会影响成本,因此请参考零件拆份部份以获得有用的指导。

Figure 1: Layout For Effective Use Of Space 有效利用空间布局



Part size is an important consideration in cost control. In Figure 1, part size is 146 x142mm (5.75" x 5.59") and panel utilization is 90%. This high utilization was achieved by reducing part size from the original 146 x 145mm (5.75" x 5.71") - only a 3mm change. The result is an increase in parts per panel from 8 to 12 utilizing the same amount of material (30% gain in panel utilization).

零件尺寸是成本控制中的重要考虑因素,在图1中,零件尺寸为146*142mm,拼板尺寸利用率为90%,达到了如此高的利用率从原始的146*145mm减少零件尺寸-仅改变3mm结果是,使用相同数量的铝可以使每块拼板的零件数量从8个增加到12个。材料(拼板利用率提高30%)。

Surface Finish

- White is the most commonly used soldermask color in the industry, and as a result it is the most cost-effective.
 Other colors such as black, green, red and blue are also available.
- If possible, try to include legend (nomenclature) in the soldermask design. Offering white and black nomenclature.
- Regarding solder pad finish, HASL and Pb-free HASL are the most cost-effective finishes. Other surface finishes such as Immersion Tin or Silver, ENIG, Ag, ENEPIG (for gold wire bond surfaces), and OSP (in panel and array form only) are available.
- Mankun's StabiLUX is a non-silicone coating that is color and UV stable, even after exposure to multiple solder reflow processes. The white product is screen coated over a solder mask allowing for optimum visual performance, even with continued use.

表面处理

- 白色是我们最常用的阻焊剂颜色,因此它是最具有成本效益的。也可以使用其他颜色,例如黑色,绿色红色和蓝色。
- 如果可以,请尽量在图纸中标记图纸(名称),阻焊层设计。字符提供露基板工艺。
- 关于焊盘的光洁度,有铅锡和无铅锡是最划算的焊盘工艺。其他表面处理例如沉银,沉金,电银,电金和防氧化(仅用于表面的阵列形式)。
- 满坤使用一种非有机硅涂料,即使暴露于多种回流焊工艺后也具有颜色和紫外线稳定性。白色产品在阻焊膜上进行了丝网涂装,即使连续使用也能获得最佳视觉效果。

Baseplate Finish

- When using aluminum, a brushed finish is typical. Other finishes like anodize and chemical conversion are available for additional cost. With copper, a brushed finish is also typical but may oxidize from handling and atmospheric conditions. Other finishes like bright electroless nickel, ENIG and/or ENEPIG are available to prevent oxidation but will drive cost up.
- When considering finishing the part edge and/or through hole edge, please note that an unfinished edge is more economical.

底板表面处理

- 使用铝时,通常使用拉丝表面处理。 其他表面处理,例如防氧化和化学转化需要支付额外费用。 对于铜做拉丝表面处理也是很典型的,但可能会做防氧化 处理,还可以使用其他光洁剂,例如光亮的化学镍等,以 防止氧化,但会增加成本。
- 如果可以,请尽量在图纸中包含图纸(名称),阻焊层设计。提供露基板命名法。
- 当考虑精加工零件边缘或通孔边缘时,请注意不加工的边缘更为经济。



PART FABRICATION

零件制造

V-Scoring

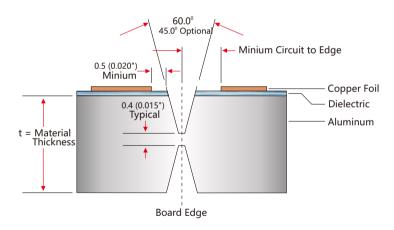
V-scoring is a viable process selection for both low and high volume production because it allows for maximum material utilization. V-scoring is also a preferred process for prototypes with rectangular geometries having the benefit of no tooling costs. Holes can be drilled or punched prior to scoring. Typical tolerance for part size, hole position to part edge, and circuit to edge is +/-0.25mm (0.010''). V-scoring is a great alternative for arrays. Circuit to edge spacing can be reduced over a typical blanked part (see Section 1.4 on page 8 of this document).

V-CUT

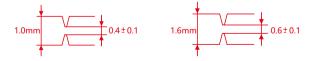
V-CUT是实现小批量和大批量生产的可行工艺选择,因为它可以最大限度的提高产量,材料利用率,对于具有矩形几何形状的原型,V刻痕也是一种优选的方法,它具有无工具成本的优势。刻痕之前可以先钻孔或打孔。零件尺寸,到零件边缘的孔位置以及到边缘的电路的典型公差为+/-0.25mm。V-CUT是数组的绝佳替代选择。可以在典型的空白部份上减少电路到边缘的间隔。

Figure 2: V-Scoring Guidelines

图2: V-CUT参考数据



一般为双向V-CUT(备注:横向)



特殊为单向V-CUT(备注:纵向)

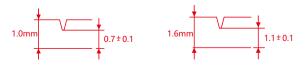
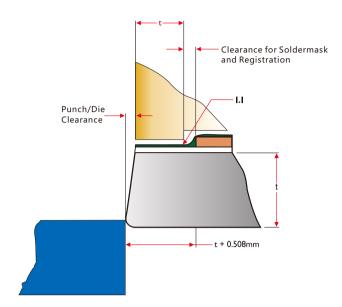


Figure 3: Punch To Die Clearance

图3: 冲模间隙



Hole Piercing / Perimeter Blanking

Hole piercing and perimeter blanking are some of the most cost effective processes for moderate to high volume applications. Blank tooling can accommodate complex part geometries and can be held to very tight tolerances. In addition to blanking the part perimeter, piercing patterns of internal holes can be produced with the most accuracy and the greatest degree of repeatability. Mankun, tclad that is to be blanked in production should be considered as early in the design process as possible. Part design is critical to ensure blanking feasibility as there are specific guidelines to be considered. Each design should be evaluated to the recommendations defined in this document prior to beginning the tool planning process (see Section 1.3 on page 8 of this document).

冲孔/零件外形冲模

冲孔和外形冲模是适用于大批量生产的最具有成本效益的工艺。 冲压模具可以容纳复杂的零件几何图形,并且可以做到小公差。 除了覆盖零件周长之外,还可以以最高精度和最大程度的重复性 制造内部孔的穿孔图案。但是,应尽可能早地考虑在生产过程中 要消除的覆铜板。零件设计是对于确保落料可行性的至关重要, 因为要考虑到具体准则,在开始规划过程之前,应根据本文定义 的建议对每种设计进行评估。

Milling

Milling processes are typically used for prototype or low volume production with complex geometries. These processes are typically not cost-effective for moderate to high volume applications.

CNC

锣工艺通常用于具有复杂几何形状的原型或小批量生产。 对于中等量到大批量应用,这些过程通常不具备成本效益。



Circuit To Edge

When planning to blank a part perimeter, the distance between the circuit pattern and the part edge is critical. To allow for sufficient relief for the circuitry, the standard minimum distance from circuit to part edge is one material thickness plus 0.5mm (0.020"). If the circuit foil is 2 oz. or thicker, the face of the perimeter punch must be designed to allow for uniform support around the part perimeter.

Active circuitry that needs to be isolated from the base plate should be placed a minimum of one baseplate material thickness plus 0.5mm (0.020") from the edge of the hole. If the circuit is a ground pattern, or same potential as the base plate, then the circuitry may be closer. Standard practice is to always leave a 1.3mm (0.051") relief around a pierced hole.

Note: The minimum diameter for a pierced hole is equivalent to one baseplate material thickness. Higher operating voltages may require larger clearances.

电路到边缘

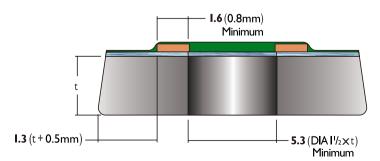
当计划遮盖零件周边时,电路图形和零件边缘之前的距离至关重要。为了给电路留出足够的空间,从电路到零件边缘的标准最小距离是一种材料厚度加上0.5mm。如果电路铜箔为2OZ或更厚的周边冲头的表面必须设计成在零件周边周围提供均匀的支撑。

需要与基板隔离的有源电路应至少放置一种基板材料厚度,再加上孔距边缘0.5mm的位置。如果电路是接地图或相同电位作为底板,则电路可能会更靠挝。标准做法是始终保留1.3mm孔周围的浮雕。

注意: 穿孔的最小直径等于一个基板材料的厚度。更高的工作电压可能需要更大的间隙。

Figure 4: Hole And Circuit To Edge Clearance 图4: 孔和线路到边缘的间隙

Cross Section View 構切断面图



Note: Use of a soldermask is recommended.

注意: 建议使用阻焊层

Radii On Corners

Punching requires that all inside and outside corners be designed with a minimum radius. It is recommended that one baseplate material thickness minimum radius be on all corners. When desired, it is possible to go down to one half baseplate material thickness radius. Mankun, this requires higher tooling costs.

圆角半径

冲孔要求所有内角与外角设计成最小半径。建议在所有拐角 处使用一个底板材料厚度的最小半径。如果需要,可以减少 到底板材料厚半径的一半。但是,这需要较高的工具成本。

Flatness

Part design, as well as the manufacturing process, affects flatness of a tclad board. There is also an effect from the differential coefficient of thermal expansion between the circuit and the baseplate layer. That effect is determined by the base plate material selection and ratio of copper foil to baseplate thickness and the percentage of circuitry per layer.

For tclad, panel or part, there is always the potential for some bow caused by the difference in between the circuit layer and the baseplate. Flatness can be further optimized by using copper base metal instead of aluminum and with proper overall design. Generally, if the thickness of the copper layer is less than 10% of the baseplate thickness, the aluminum will be mechanically dominant. Constructions with more circuit copper than 10% of the baseplate thickness can exhibit a bow. Copper foil thicknesses less than 10% of the baseplate thickness can be controlled well within IPC specifications. Flatness can be further optimized with proper tool design and/or additional processing.

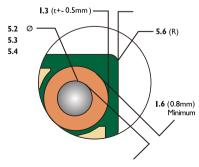
平整度

零件设计以及制造过程都会影响覆铜板的平坦度。电路和基 板层之前的热膨胀系数差异也有影响。该效果取决于基板材 料的选择和比例,铜箔与基板的关系以及每层电路的百分比。

对于覆铜板,拼板或零件,电路层和基板之间的差异始终会导致某些弯曲。通过使用铜基金属代替铝并具有适当的整体设计,可以进一步优化平面度。通常,如果铜层的厚度小于基板厚度的10%,则铝会以机械方式支配。电路铜超过基板厚度的10%的结构可能会出现弯曲。铜箔厚度小于基板厚度的10%,可以在IPC规范内很好的控制,平坦度可以通过适当的工具设计或附加处理来进一步优化。

Planned View 平面图







TESTING OPTIONS

测试选项

Electrical Opens And Shorts

- 1. For single-layer boards using A.O.I. (Automatic Optical Inspection) is the most cost-effective method. Using original Gerber data to compare to the etch panel will find any anomalies, even in an etch-down condition.
- 2.The more traditional "Bed-of-Nails" testing is also available. This requires a fixture charge and is a higher cost method. It is the only viable method for two-layer constructions.

电气开路和短路

- 1.对于使用AOI(自动光学检查)的单层板,这是最经济的方法。使用原始Gerber数据与蚀刻面板进行比较,即使在蚀刻条件下,也会发现任何异常情况。
- 2.还可以使用更传统的"飞针"测试。这需要固定费用,并且 是成本较高的方法,这是用于双层结构唯一可行方法。

Proof Testing (HiPot)

Testing is done to verify dielectric strength integrity of a tclad board.

- 1. Proof testing done in panel form is the most costeffective method. This form of testing is done at postetch condition, prior to surface finish or final fabrication.
- 2. The recommended method for safety agency requirements on tclad assemblies is an individual piece-part or array-part test. This method 100% tests and marks each finished board and/or array. This method requires a fixture charge.
- 3. When higher test voltages are required to meet safety agency requirements; standard clearances for fabrication may not be enough to allow for "Creepage Clearance" to meet test voltages. These minimum creepage distances can be found in safety agency standards or IPC-2221 for reference.

测试架测试 (HiPot)

完成测试以验证金属基板的介电(绝缘)强度的完整性。

- 1.以拼板形式进行测试架测试是最具有成本效益的方法。这 种测试形式是在蚀刻后的条件下进行的。然后进行表面精 加工或最终制造。
- 2.针对覆铜板组件的安全机构要求的推荐方是单个零件和 拼板零件测试。此方法100%测试并标记每个成品板或拼 板,此方法需要固定装置费用。
- 3.当需要更高的测试电压以满足安全机构的要求时,制造的标准间隙可能不足以允许"漏电间隙"满足测试电压。这些最小漏电距离可在安全机构标准或IPC-2221中找到,以供参考。

ADVANCED CIRCUIT PROCESSING

高级电路处理

Part Forming

Tclad is designed with a copper or aluminum baseplate that can be formed. In order to maintain thermal and electrical integrity, circuits cannot go across the formed area.

电气开路和短路

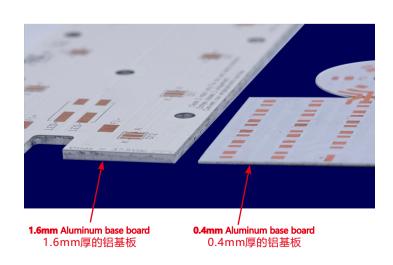
铝基覆铜箔层压板设计有可以形成的铜或铝基板。为了保持 热和电气的完整性,电路不能穿过成型区域。

Ultra Thin Circuits

Ultra Thin Circuits (UTC) utilize tclad dielectrics without the typical thick base layer. These circuits are often used for component level packaging where the thick aluminum or copper base is not required for mechanical or thermal mass. The circuit layer can be a "stand-alone" ceramic submount replacement. The total profile of a UTC can be as thin as 0.23mm (0.009") and can be used in double-sided structures.

超薄电路

超薄电路(utc)使用不带衬垫的电介质而没有典型的厚基层。 这些电路通常用于组件级封装,其中机械或热质量不需要厚的铝或铜基板。电路层可以是"独立"陶瓷底座的替代品。 UTC的总轮廓可薄至0.23mm,可用于双面结构。





2-LAYER DESIGN CONSIDERATIONS

双层设计注意事项

Benefits And Considerations

Tclad dielectrics in 2-layer constructions have significant benefits in overall design when compared to 2-layer FR-4 constructions. These benefits include; higher power density, electromagnetic shielding and/or improved capacitive coupling. While designing your 2-layer circuit, please keep these items in mind:

- •Inner layer copper thickness is limited to 140 micron (4 oz.) before plating.
- •Due to the lower thermal impedance of tclad dielectric as compared to FR-4, thermal via's are not usually required. However, if thermal via's are used better thermal performance can be achieved.
- •When using a copper base plate, connections from the circuits to the baseplate are possible using a plated Blind-via or thruhole.
- •Using electrical/thermally conductive via fill materials and overplating with copper creates a flat surface area enabling solderable pads for devices eliminating solder voiding.
- A selective dielectric removal process can be used to expose the inner-layer and/or the baseplate for component attachment to these layers if desirable. This type of design reduces thermal resistance.

好处和注意事项

与两层FR-4结构相比,两层结构中的包覆电介质在总体设计上具有显著优势。这些好处包括:更高的功率密度,电磁屏蔽或改善的电容耦合。在设计两层电路时,请牢记以下几点:

- 电镀前,内层铜的厚度限制为140微米 (4OZ).
- 由于与FR-4相比,覆层介质的热阻抗较低,因此通常不需要散热孔。但是,如果使用散热孔,则可以实现更好的散热性能。
- 当使用铜基板时,可以使用电镀的盲孔或通孔将电路连接到基板。
- 使用导电/导热通孔填充材料并镀铜会产生平坦的表面积,从而 使器件的可焊接的垫片用于消除焊料漏气的装置。
- 如果需要可以使用选择性介电去除过程来暴露内层或基板以便 将组件连接到这些层。这种类型的设计降低了热阻。

Material Selection And Fabrication

2-layer designs incorporate additional amounts of copper and dielectric thickness over single-layer designs. As a result, additional considerations must be made with regard to material construction choices and fabrication.

- •Flatness is affected by the amount of copper so CTE rules must be considered in the equation. Most heavy copper constructions will require a thicker aluminum base substrate or copper base to prevent bowing.
- •The additional dielectric thickness will also create the need for larger minimum distances in drilling, scoring, routing and punching. See the section regarding fabrication.
- •Copper plating adds approximately 1 oz. to the copper foil layer.

材料选择与制造

双层设计比单层设计包含更多的铜和介电厚度。因此,必须 在材料构造选择和制造方面作出更多考虑。

- 平坦度受铜量的影响,因此必须在设计中考虑CTE规则。 大多数较重的铜结构都需要较厚的铝基底或铜基底,以防止弯曲。
- 额外的介电层厚度还将导致钻孔,V割,布线和冲压中需要 更大的最小距离。
- 铜箔层增加镀铜大约1OZ。



DESIGNING A NON-RECTANGULAR PART ARRAY

设计非矩形零件拼板

Comparing An Array In Three Different Considerations

Non-rectangular designs typically require additional spacing in the array for milling or punching the shape. Often a combination of scoring and milling/punching is required to create the part shape and allow parts to be separated from the array after assembly. Additional process steps and reduced material utilization can impact cost.

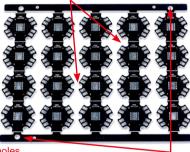
三种不同的考虑

非矩形设计通常需要在拼板中留出额外的间距以V割或冲压成形状。通常需要将V割和锣/冲孔结合来创建零件形状,并允许零件拼板后与工作边分离。额外的处理步骤和材料利用率的降低会影响成本。

Figure 11: Original Array Design

图11: 原始的拼板设计

Parts spaced apart, lack of common score lines 零件间隔开,缺少共同的刻痕线



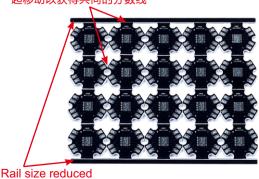
Large rails with pin holes 带针孔的大工作边

Figure 12: Improved Design

工作边尺寸减少

图12: 改进的设计

Parts moved together for common score lines 零件一起移动以获得共同的分数线



Design Considerations For Better Material Utilization

Are rails required for assembly? Rails consume material that will be discarded after parts are separated from the array. When designing an array, size and number of rails should be considered to optimize panel utilization. The reduced rail design in Figure 12 below uses less material than the one in Figure 11, and even less material is required for the design with no rails in Figure 13.

Will assembled components require parts to be spaced further apart? This can result in multiple score lines and reduced material utilization. Consider part orientation in the array. Alternating orientation may allow components to nest, maximizing material utilization. In the original array design (Figure 11), parts are spaced further apart and use more material as compared to the common score lines used in the improved and optimized designs (Figures 12 and 13).

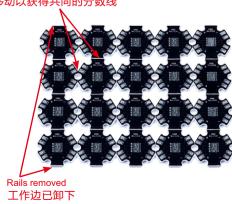
设计注意事项以提高材料利用率

- 拼板需要工作边吗?工作边消耗的材料会在零件与阵列分离后被丢弃。设计拼板时,应考虑工作边的尺寸和数量以优化基板利用率。下图12中的精简设计使用的材料比图11中的材料更少,更少的材料如图13中没有工作边的设计。
- 拼板后的零件是否需要将零件分开放置?这可能导致多个 V割线并降低材料利用率。考虑拼板中的零件方向,交替 的方向可以使组件嵌套,从而最大程度的利用材料。在原 始拼板设计(图11)中,与改进和优化设计(图12和13)中使用的通用V割线相比,零件之间的距离更远并且使用 的材料更多。

Figure 13: Optimized Design

图13: 优化的设计

Parts moved together for common score lines 零件一起移动以获得共同的分数线





Design Type 设计类别	Design Parameter 设计参数	Standard Design Recommendation 标准设计建议和规范	Standard Design Recommendation and Specification 标准设计建议和规范				
1.0 Circuit Design 电路设计		CIRCUIT THICKNESS 电路铜厚	MINIMUM LINE WIDTH 最小线宽				
	4445	35μm (1 oz)	0.13mm (0.005")				
	1.1 Minimum Circuit Width 最小电路宽度	70μm (2 oz)	0.15mm (0.006")				
		105μm (3 oz)	0.18mm (0.007'')				
		140μm (4 oz)	0.20mm (0.008")				
		1-LAYER (NON-PLATED) 单层 (非镀)	2-LAYER (PLATED) 双层 (镀)				
	1.2 Minimum Space and Gap Single and Double Layer	35µm (1 oz) - 0.18mm (0.007'')	35µm (1 oz) - 0.23mm (0.009'')				
		70μm (2 oz) - 0.23mm (0.009'')	70μm (2 oz) - 0.30mm (0.012'')				
	单层、双层 最小空间间隙	105μm (3 oz) - 0.30mm (0.012")	105μm (3 oz) - 0.36mm (0.014'')				
		140µm (4 oz) - 0.36mm (0.014")	140µm (4 oz) - 0.41mm (0.016'')				
	1.3 Minimum Circuit to Edge Blanking 最小蚀刻电路	One baseplate material thickness + 0.5mm (0.20") 一个基板材料厚度+ 0.5mm (0.20")					
	1.4a Minimum Circuit to Edge, V-Scored V-CUT 最小刻痕厚度	MATERIAL THICKNESS 材料厚度 1.0mm (0.040'') 1.6mm (0.062'') 2.0mm (0.080'') 3.2mm (0.125'')	CIRCUIT TO EDGE DISTANCE 电路到边缘距离 0.66mm (0.026") 0.74mm (0.029") 0.79mm (0.031") 0.94mm (0.037")				
	1.4b Minimum Circuit to Edge, Milled V割到边的最小电路	0.5mm (0.020")					
	1.5 Minimum Conductor to Hole Edge 孔边缘的最小导体	One baseplate material thickness 一块底板厚度					
	1.6 Copper Land w/Non-Plated Through Holes 铜焊盘,带/ 非电镀通孔	Punched non-plated thru-hole is 0.76mm (0.030'') minimum 冲孔非电镀通孔的最小为0.76mm					
	1.7 Minimum Character Height for Etched 刻蚀最小字符高度(取决于铜箔厚度)	1.5mm (0.060'')					
2.0 Soldermask Design 阻焊设计	2.1 Minimum Soldermask Line Width 最小阻焊层宽度	0.20mm (0.008'')					
	2.2 Minimum Soldermask Aperture 最小阻焊层孔径	0.20mm x 0.20mm (0.008" x 0.008")					
	2.3 Minimum Character Height and Line 最小字符高度和线条	1.50mm x 0.25mm (0.060" x 0.010")					
	2.4 Soldermask Color 阻焊油颜色	Green, White, Black, Red, Blue are available 绿色,白色,黑色,红色,蓝色等都可以 Minimum character height / Minimum line width 0.25mm (0.010")					
	2.5 Character Height / Width (In Soldermask) 字符高度/宽度(在阻焊层中)	最小字符高度/最小线宽0.25mm					
3.0 Legend Design 传统设计	3.1 Nomenclature to Pad (Ink Jet Printing) 丝印/ 移印 (喷墨打印)	推荐最低从命名功能至最近的焊盘的距离为0.2	Recommended min. distance from nomenclature feature to nearest pad is 0.25mm (0.010") 推荐最低从命名功能至最近的焊盘的距离为0.25mm				
	3.2 Character Height / Width 字符高度/宽度	1.0mm (0.040") minimum height, 0.15mm (0.006") minimum width 最小高度为1.0mm,最小宽度为0.15mm Same as circuit distance					
	3.3 Minimum Distance to Board Edge 到板边缘的最小距离 3.4 Nomenclature Color	与电路距离相同					
	字符标识颜色	White and black 白色和黑色					
4.0 Surface Finish 表面处理	4.1 Surface Finish Available 可用的表面处理	Lead-free HASL, tin-sinking,tin-plating,nickel-plating,gold-plating,gold-sinking,OSP 无铅喷锡,沉锡,镀镍,镀金,沉金,防氧化等					
5.0	5.1 Hole to Board Edge 孔到板边缘		Min. distance from edge of hole to edge of board is one baseplate material thickness 从孔的边缘到板的边缘的距离是一块底板材料的厚度				
Mechanical Design 机械设计	5.2 Punched Hole Size 冲孔尺寸	Minimum punched hole size is 1.5x base 最小打孔尺寸是基板材料厚度的1.5倍。	Minimum punched hole size is 1.5x baseplate material thickness 最小打孔尺寸是基板材料厚度的1.5倍。				
	5.3 Minimum Drilled Hole Diameter - Copper Baseplate 铜基板最小钻孔直径	One baseplate material thickness 一块底板材料厚度					
	5.4 Minimum Drilled Hole Diameter - Aluminum Baseplate 铝基板最小钻孔直径	MATERIAL THICKNESS 材料厚度 1.0mm (0.040") 1.6mm (0.062") 2.0mm (0.080") 3.2mm (0.125")	DRILLED HOLE DIAMETER 钻孔直径 0.76mm (0.030") 0.76mm (0.030") 1.0mm (0.040") 1.6mm (0.062")				
	5.5 Minimum Drilled Via Diameter for Circuit Layer (Foil Thickness Dependent) 电路层的最小通孔,直径(取决于铜箔厚度)	0.25mm (0.010'')	0.25mm (0.010")				
	5.6 Minimum Edge Radius 最小边缘半径	One baseplate material thickness for blanking, no radius for V-scoring 一块底板材料厚度,用于V割刻的半径					



- Guideline 1.3:The minimum circuit to edge blanking distance allows the punch to engage the metal baseplate and dielectric without damaging adjacent circuitry and improves tool life. 最小的电路边缘的冲栽距离允许冲床与金属基板和电介质接合,而不会损坏相邻电路并提高刀具寿命。
- Guideline 1.4: The minimum distance from circuit to edge must be met to provide isolation from the circuitry to the baseplate. Note: Additional distance from circuit to hole may be required depending on application and proof testing requirements.

必须满足从电路至边缘的最小距离,以便从电路到基板的隔离。注意:根据应用和验证测试要求视具体情况而定,可能需要从电路到孔的额外距离。

Guideline 1.5: The minimum conductor to hole edge distance must be achieved to provide isolation from circuitry to the base.

必须达到导体到孔边缘的最小距离,以便从电路到基座的隔离。

- Guideline 1.7:The minimum character height for etched nomenclature must be met for optimum legibility. (中國工序的最小字符高度必须达到最佳易读性。
- Guideline 2.1:Minimum soldermask line width is needed for proper adhesion of the soldermask to the board surface. This is also an important consideration for maintaining separation between pads (solderdams).
 - 为了使阻焊层与电路板表面适当粘合,需要最小的阻焊层线宽,这也是保持焊盘(焊锡)之间间距的重要考虑因素。
- Guideline 2.2: Solder pad apertures designed with overlap ensure proper adhesion of the soldermask to the board surface and prevention of exposure to copper and bridging between features. 有重叠设计的焊盘、焊锡孔,间隙以确保焊锡面与板表面的适当粘合,并防止暴露铜和零件之间短路。
- Guideline 2.3: The minimum soldermask specification keeps the pads exposed so they can accept the surface plating and ensures the pad will remain large enough to be functional. 最小的焊锡面规格使焊盘保持裸露,以便它们可以接受表面电镀,并确保焊盘足够大尺寸以发挥作用。
- Guideline 2.4: A standard minimum character height and width is set to ensure legibility. 标准的最小字符高度和宽度,以确保易读。
- Guideline 3.1: A character width and height are specified for silk screening to assure legibility and adhesion. 为丝印规定了字符宽度和高度,以确保易读性和粘和性。
- Guideline 3.2: The minimum distance from silk screen to the nearest pad is required for registration to keep the legend ink off of solderable surfaces.

标记从丝网到最近的板子的最小距离,以使图案油墨远离焊盘表面。

- Guideline 3.3: A minimum distance to board edge is specified to ensure clearance for punch land, for registration purposes and to maintain legibility.

 标记的目的是为了保持易辨性,规定了到板边缘的最小距离,以确保冲床打孔的间隙。
- Guideline 5.1: The minimum distance from hole edge to board edge is important to avoid material distortion during processing.

 从孔边缘到板边缘的最小距离对于避免加工过程中的材料变形很重要。
- Guideline 5.2: A minimum punched hole size is recommended to ensure tool strength integrity during processing and to avoid premature tool wear.

 建议最小打孔尺寸,以确保加工过程中工具强度的完整性,并避免工具过早磨损。
- Guideline 5.3: A minimum drilled hole diameter for the copper baseplate is in place to ensure tool strength integrity during processing and to avoid premature tool wear.

 [铜基板的最小钻孔直径到位,以确保加工过程中工具强度的完整性并避免工具过早磨损。
- Guideline 5.4: The aluminum baseplate has a minimum drilled hole diameter specification to ensure tool strength integrity during processing and to avoid premature tool wear.

 田基板具有最小钻孔直径规格,以确保加工过程中工具强度的完整性并避免工具过早磨损。
- Guideline 5.5: The circuit layer's recommended minimum drilled via diameter ensures tool strength integrity during processing and helps to avoid premature tool wear.

 建议的电路层最小钻孔直径以确保加工过程中工具强度的完整性,并避免工具过早磨损。

The above-mentioned content Mankun's circuit processing capabilities.

If your application requires different specifications, please contact your Mankun Sales Representative.

以上內容代表满坤电路的处理能力,如果您的产品要求需要不同的规格,请联系您的销售代表。

满坤电子有限公司 MANKUN ELECTRONIC CO., LTD.

Add: No.40 Shinan Street, Dawen Village, Dongchong Town, Nansha District, Guangzhou City, China. P.C.: 511453

Web: www.mankun.net/www.mankun.net.cn Tel: +86-20-3483-2899 Fax: +86-20-8072-0030 Mob: 133 9261 9948 E-mail: bellum@mankun.net



